REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 6 and 7 have been amended. Claims 11-29 have been previously withdrawn from consideration. Thus, claims 1-10 are currently pending in the application and subject to examination.

Rejection Under 35 U.S.C. § 103(a)

In the outstanding Office Action, claims 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Preiss et al., U.S. Patent No. 6,757,763 (hereinafter, "Preiss") and further in view of Gulick, U.S. Patent No. 5,898,848 (hereinafter, "Gulick"). It is noted that claims 1, 6 and 7 have been amended. To the extent that the rejection remain applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

In the Applicants' invention as recited in independent claim 1, as amended, a buffer stores only communication data sent from a first device connected to a first bus and a register stores only communication control information concerning the communication data sent from the first device for handling the communication data. When writing of the communication data is completed, data end information is written as the communication control information. A control circuit passes the communication data stored in the buffer to a second device connected to the second bus, and passes the communication control information stored in the register to the second device, wherein the communication control information and the communication data are sent via the register and the buffer, respectively, and the second device performs an appropriate

receive process according to the control information and completes the receive process when detecting the data end information.

In the Applicants' invention as recited in independent claim 6, as amended, a first buffer stores only first communication data sent from a first device connected to a first bus and a first register stores only first communication control information concerning the first communication data sent from the first device for handling the communication data. When writing of the first communication data is completed, data end information is written as the first communication control information. A second buffer stores only second communication data sent from a second device connected to a second bus and a second register stores only second communication control information concerning the second communication data sent from the second device for handling the communication data. When writing of the second communication data is completed, data end information is written as the second communication control information. A control circuit passes the first communication data stored in the first buffer to the second device and the first communication control information stored in the first register to the second device, and further passes the second communication data stored in the second buffer to the first device and the second communication control information stored in the second register to the first device, wherein the first and second communication control information are sent via the first and second registers, respectively, and the first and second communication data are sent via the first and second buffers, respectively, and the first device and the second device perform an appropriate receive process according to the second and first control information, respectively, and complete the receive process when detecting the data end information.

In the Applicants' invention as recited in independent claim 7, as amended, a receive buffer stores only receive data received from said external host apparatus and a receive register stores only receive communication control information concerning the receive data from an external host apparatus for handling the receive data, and when the receive data ends, data end information is written as the receive communication control information. A transmit buffer stores only transmit data transmitted from an internal CPU via an internal bus and a transmit register stores only transmit communication control information concerning the transmit data from the internal CPU for handling the transmit data, and when writing of the transmit data is completed, data end information is written as the transmit communication control information. A control circuit for passing the receive data stored in the receive buffer to said internal CPU and passing the receive communication control information stored in the receive register to the internal CPU, and further passing the transmit data stored in he transmit buffer to the external host apparatus and passing the transmit communication control information stored in the transmit register to the external host apparatus, wherein the receive data and receive communication control information are sent via the receive buffer and receive register, respectively, and the transmit data and transmit communication control information are sent via the transmit buffer and transmit register, respectively, and wherein the internal CPU and the external host apparatus perform an appropriate process according to the control information and complete the process when detecting the data end information.

Thus, in the claimed invention, data end information is transferred as control information.

In the outstanding Office Action, the Examiner admits that Preiss fails to disclose storing the communication control information in a register and transferring the communication data (stored in the buffer) in addition to the communication control information (stored in the register) to the designation device. See, *Office Action*, pp. 2-3.

Gulick is cited as allegedly curing the admitted deficiency of Preiss. In particular, the Examiner asserts that Gulick teaches storing "transfer information" in a target address register 5076 of Fig. 17 and storing only communication data in a data buffer 5074 of Fig. 17. See, *id.*, p. 3.

However, the "transfer information" stored in the target address register 5076 of Fig. 17 of Gulick is a target address. See, *Gulick* at, e.g., col. 16, lines 34-36. As explained above, in the claimed invention, when writing of the communication data is completed, data end information is written as the communication control information making it possible to recognize an end point without analysis of communication data. As a result, efficient data reception can be realized by the claimed invention.

Neither Preiss nor Gulick, alone or combined, discloses or suggests at least the features of claims 1, 6 and 7 noted above. For at least this reason, the Applicants submit that claims 1, 6 and 7 are allowable over the applied art of record. As claims 1, and 7 are allowable, the Applicants submit that claims 2-5 and 8-10, which depend from allowable claims 1 and 7, respectively, are likewise allowable for at least the reasons set forth above with respect to claims 1 and 7.

Conclusion

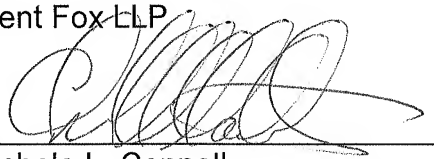
For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 107337-00106.

Respectfully submitted,

Arent Fox LLP



Michele L. Connell
Registration No. 52,763 25,895

Customer No. 004372
1050 Connecticut Ave., N.W.
Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 857-6104
Facsimile No. (202) 857-6395

MLC:cdw

Enclosures: Request for Continued Examination
Petition for Extension of Time